

4th IEEE International Workshop on Infrastructure IP (I-IP 2006)

Claremont Resort, Berkley, California, USA

May 3-4, 2006

Held in conjunction with [VLSI Test Symposium, 2006](#)

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Call for Papers

Scope

The higher level of manufacturing susceptibility and field reliability in today's SoC require enhanced detection, diagnosis and yield optimization solutions. These solutions necessitate incorporating on-chip infrastructure IP blocks, in addition to the functionality of the SoC. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This workshop analyzes this key trend and gives the chance to describe a range of infrastructure IP for today's System-on-Chip (SoC) designs. This includes infrastructure IP for test, diagnosis, timing measurement, debugging, test, repair, and fault tolerance.

Areas of Interest include but are not limited to

- *Embedded diagnosis IP*
- *Design for Manufacturability*
- *Built-in Repair Analysis and Built-in Self-Repair*
- *Yield enhancement IP*
- *Built-in monitors and embedded measurement functions*
- *Embedded Test solutions (BIST)*
- *On-line error detection and correction blocks*
- *Transient error protection hardware*
- *Process monitoring IP*
- *Silicon debug infrastructure*

Author information

To present at the Workshop, authors are invited to submit paper proposals. The proposals may be extended abstracts (1,000 words) or full papers. Each submission should include: title, full name and affiliation of all authors, an abstract of 50 words, and keywords. Also, identify a contact author and include a complete correspondence address, phone number, fax number, and e-mail address.

Submit a copy of your paper proposal by Postscript, or PDF, via E-mail. Proposals for panel discussions are also invited. Submissions are due no later than **March 11, 2006**.

Submit your paper proposal to:

- Dimitris Gizopoulos, Piraeus U, digizop@unipi.gr, Tel: +30-210-414-2372

Authors will be notified of the disposition of their papers by **March 30, 2006**.

Authors of accepted papers may submit an illustrated text by **April 10, 2006** for inclusion in the Digest of Papers, which will be provided to the attendees.

I-IP 2006 is sponsored by the IEEE Computer Society Test Technology Technical Council.

For more information on I-IP 2006, visit the workshop website at:

<http://www.unipi.gr/iip>

