

WORKSHOP LOCATION

I-IP 2005 will be held at the Lodge at Rancho Mirage, Palm Springs, California, USA, May 4-5, 2005, immediately following VTS 2005 (<http://www.tttc-vts.org>).

REGISTRATION

All workshop participants require registration. Please register using the VTS 2005 Registration Forms.

INFORMATION

For more information on the Workshop, please contact:

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WORKSHOP COMMITTEE

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I-IP 2005

3rd IEEE International Workshop on
Infrastructure IP

<http://www.unipi.gr/iip>

The Lodge at Rancho Mirage
Palm Springs, California, USA
May 4-5, 2005

TECHNICAL PROGRAM

Sponsored by -

*TTTC - The IEEE Computer Society Test
Technology Technical Council*

In Conjunction with -

*IEEE VLSI Test Symposium 2005
(VTS 2005)*

WORKSHOP SCOPE

The higher level of manufacturing susceptibility and field reliability in today's SoC requires enhanced detection, diagnosis and yield optimization solutions. These solutions necessitate incorporating on-chip infrastructure IP blocks, in addition to the functionality of the SoC. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This workshop analyzes this key trend and gives the chance to describe a range of infrastructure IP for today's System-on-Chip (SoC) designs. This includes infrastructure IP for test, diagnosis, timing measurement, debugging, test, repair, and fault tolerance.

WORKSHOP AT A GLANCE

Wednesday, May 4th, 2005

2:00 pm - 5:00 pm	Registration
4:00 pm - 4:15 pm	Opening Session
4:15 pm - 6:15pm	Session 1: Infrastructure IP for Yield and Reliability
7:00 pm - 9:00 pm	Evening Reception

Thursday, May 5th, 2005

7:00 am - 8:00 am	Continental Breakfast
8:00 am - 10:00 am	Session 2: Embedded I-IP for Measurement, Characterization and Manufacturing Test
10:00 am - 10:30 am	Break
10:30 am - 12:00 pm	Session 3: Is Silicon Debug the Cinderella of I-IP?
12:00 pm - 2:00 pm	Lunch
2:00 pm - 4:00 pm	Session 4: Advanced I-IP Solutions for Test Complex SoCs

PROCEEDINGS

Informal Digest will be made available to all attendees. This will include extended abstracts, summaries or papers optionally provided by authors based on their presentations.

WEDNESDAY, MAY 4TH, 2005

REGISTRATION 2:00 pm - 5:00 pm

OPENING ADDRESS 4:00 pm - 4:15 pm

Welcoming Remarks

Y. Zorian, General Chair
D. Gizopoulos, Program Chair

Session 1: 4:15 pm - 6:15 pm

INFRASTRUCTURE IP FOR YIELD AND RELIABILITY

Moderator: R.Aitken—ARM

- 1.1 Soft Error Radiation Test, Simulation, and Protection in Nanometer Technologies, E.Dupont, M.Buehler-Garcia—iRoC Technologies
- 1.2 Concurrent On-Line Testing of Identical Finite-State Machines Using Non-Identical Input Sequences, I.Pomeranz—Purdue U., S.M.Reddy—U.Iowa
- 1.3 Infrastructure IP for Yield Optimization, G.Yeric—HPL

DISCUSSION PANEL

RECEPTION 7:00 pm - 9:00 pm

THURSDAY, MAY 5TH, 2005

CONTINENTAL BREAKFAST 7:00 am - 8:00

Session 2: 8:00 am - 10:00 am

EMBEDDED I-IP FOR MEASUREMENT, CHARACTERIZATION AND MANUFACTURING TEST

Moderator: A.Ivanov—UBC

- 2.1 Maximizing DfM for IP Blocks, Y.Zorian—Virage Logic
- 2.2 ATE Design Considerations to support High-Speed I/O BIST and applications proliferation, S.Wigley, M.Mowji—LTX
- 2.3 Survey of Infrastructures for Mixed-Signal IP Test, S.Tabatabaei—Virage Logic

DISCUSSION PANEL

COFFEE BREAK 10:00 am - 10:30 am

Session 3: 10:30 am - 12:00 pm

IS SILICON DEBUG THE CINDERELLA OF I-IP?

Co-Organized with:

IEEE
Design&Test
of Computers

Organizer:

M.Abramovici—DAFCA

Moderator:

R.Chandramouli—Virage Logic

Panelists:

C.J.Clark—Intellitech

M.Ricchetti—ATI

S.Venkataraman—Intel

M.Abramovici—DAFCA

D.Appello—ST Microelectronics

LUNCH 12:00 pm - 2:00 pm

Session 4: 2:00 am - 4:00 pm

ADVANCED I-IP SOLUTIONS FOR TEST COMPLEX SOCS

Moderator: TBD

- 4.1 STESI: Testing Wrapped IP Cores using a dedicated Test Processor, M.Tuna, M.Benabdendi, A.Greiner—LIP6
- 4.2 Towards an IEEE P1500 Verification Infrastructure, A Comprehensive Approach, I.Diamantidis, T.Oikonomou, S.Diamantidis—Globetech Solutions
- 4.3 Methodologies and Algorithms for Testing Switch-based NoC Interconnects, C.Grecu, P.Pande, B.Wang, A.Ivanov—UBC

DISCUSSION PANEL