

WORKSHOP LOCATION

I-IP 2004 will be held at the Charlotte Convention Center, Charlotte, North Carolina, USA, October 28-29, 2004, immediately following ITC 2004 (www.itctestweek.org).

REGISTRATION

All workshop participants require registration. Please register using the ITC 2004 Registration Forms.

INFORMATION

For more information on the Workshop, please contact:

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or <http://computer.org/ttcc>

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I-IP 2004

2nd IEEE International Workshop on Infrastructure IP

<http://www.unipi.gr/iip>

Charlotte Convention Center
Charlotte, North Carolina, USA
October 28-29, 2004

TECHNICAL PROGRAM

Sponsored by -

*TTTC - The IEEE Computer Society Test
Technology Technical Council*

In Conjunction with -

*ITC 2004 - The International Test
Conference/Test Week 2004*

WORKSHOP SCOPE

The higher level of manufacturing susceptibility and field reliability in today's SoC requires enhanced detection, diagnosis and yield optimization solutions. These solutions necessitate incorporating on-chip infrastructure IP blocks, in addition to the functionality of the SoC. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This workshop analyzes this key trend and gives the chance to describe a range of infrastructure IP for today's System-on-Chip (SoC) designs. This includes infrastructure IP for test, diagnosis, timing measurement, debugging, test, repair, and fault tolerance.

WORKSHOP AT A GLANCE

Thursday, October 28th, 2004

2:00 pm - 5:00 pm	Registration
4:00 pm - 4:30 pm	Opening Session
4:30 pm - 6:30pm	Session 1: Advanced Infrastructure IP Solutions for SoC Test, Debug and Characterization
7:00 pm - 9:00 pm	Evening Reception

Friday, October 29th, 2004

7:00 am - 8:00 am	Continental Breakfast
8:00 am - 10:00 am	Session 2: Infrastructure IP for Test & Measurement
10:00 am - 10:30 am	Break
10:30 am - 12:00 pm	Session 3: Infrastructure IP for Repair
12:00 pm - 1:00 pm	Lunch
1:00 pm - 4:00 pm	Session 4: Interface Test and Robustness IP

PROCEEDINGS

Informal Digest will be made available to all attendees. This will include extended abstracts, summaries or papers optionally provided by authors based on their presentations.

THURSDAY, OCTOBER 28TH, 2004

REGISTRATION 2:00 pm - 5:00 pm

OPENING ADDRESS 4:00 pm - 4:30 pm

Welcoming Remarks

Y. Zorian, General Chair
D. Gizopoulos, Program Chair

Session 1: 4:30 pm - 6:30 pm
ADVANCED INFRASTRUCTURE IP SOLUTIONS FOR SOC TEST, DEBUG AND CHARACTERIZATION

Moderator: C.Metra - University of Bologna

- 1.1 *On-Chip Test Infrastructure Design for High Throughput Multi-Site Testing of SoCs*, S.K. Goel, E.J. Marinissen - Philips Research
- 1.2 *Infrastructure for Testing of an Embedded Core*, T. McLaurin - ARM
- 1.3 *Supporting Debug and Test of a SoC Through an I-IP*, D. Appello, P. Bernardi, M. Grosso, M. Rebaudengo, M. Sonza Reorda - ST Microelectronics and Politecnico di Torino
- 1.4 *An Embedded Clock for SoC Path Delay Characterization*, B. Wang, D. Ho, S. Sheikhaei, A. Ivanov - U. of British Columbia

DISCUSSION PANEL

A.Khoche - Agilent, D.Appello - ST

RECEPTION 7:00 pm - 9:00 pm

FRIDAY, OCTOBER 29TH, 2004

CONTINENTAL BREAKFAST 7:00 am - 8:00

Session 2: 8:00 am - 10:00 am
INFRASTRUCTURE IP FOR TEST & MEASUREMENT

Moderator: M.Chandramouli - VirageLogic

- 2.1 *BEOL Diagnosis based on Ring Oscillator Characterization*, J.M. Portal, L. Forli, H. Aziza, D. Née, B. Borot - L2MP-Polytech-UMR CNRS and ST Microelectronics
- 2.2 *A Simple Approach to Diagnose Localized Thermal and IR Drop Effects on a Microprocessor Core Using On-Chip Synthesizable Ring Oscillators*, N. Parris, J. Healey, C. Hawkins - ARM

2.3 *Microelectronic Infrastructure for Ultra Reliable Wireless Sensor Networks*, B. Kaminska - Pultronics

DISCUSSION PANEL

S. Tabatabaei - GuideTech, M.Slamani - IBM

COFFEE BREAK 10:00 am - 10:30 am

Session 3: 10:30 am - 12:00 pm
INFRASTRUCTURE IP FOR REPAIR
Co-Organized with:

The logo for IEEE Design & Test of Computers, featuring the IEEE logo and the text "Design & Test of Computers".

- 3.1 *Infrastructure for Successful BEOL Yield Ramp, Transfer to Manufacturing, and Design for Manufacturing Characterization at 65nm and Below*, G. Yeric, E. Cohen, J. Garcia, K. Davis, E. Salem and G. Green - HPL Technologies
- 3.2 *Hierarchical I-IP Network for STAR Memory System Diagnosis*, A. Yessayan, K. Darbinyan, Y. Zorian - Virage Logic
- 3.3 *Built-In Self Repair Infrastructure IP for Compilable Embedded DRAM*, M. Nelms, D. Anand, J. Barth, J. Dreibelbis, K. Gorman, G. Pomichter, D. Pontius - IBM Microelectronics

DISCUSSION PANEL

C.Dixit - LSI Logic, M.Sonza Reorda - PdT

LUNCH 12:00 pm - 1:00 pm

Session 4: 1:00 am - 4:00 pm
INTERFACE TEST AND ROBUSTNESS IP
Moderator: A. Ivanov - UBC

- 4.1 *Reliability is No Longer a Fixed Number*, E. Dupont, M. Nicolaidis - iRoC Technologies
- 4.2 *Speedup BER Test for Multiple GB/s Ports by Infrastructure IP*, Y. Huang - Mentor Graphics
- 4.3 *Cerberus I-IP: an HW/SW approach to Control Flow Checking*, P. Bernardi, L. Bolzani, M. Rebaudengo, M. Sonza Reorda, F. Vargas, M. Violante - PUCRS and Politecnico di Torino

DISCUSSION PANEL

J. Dodge, Cadence