

2nd IEEE International GHz/Gbps Test Workshop (GTW'05)

Austin, Texas, USA

10 - 11 November 2005

Held in conjunction with [International Test Conference /Test Week](#) TM

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Call for Papers

Scope

Chips running in the multi-GHz clock ranges and/or including I/O capable of multi-Gbps data rates are now increasingly common. The characterization and production testing and diagnosis of such chips pose significant challenges. Such chip and system trends are mirrored by new trends in ATE and test methodologies. GTW'05 is a TTTC workshop that specifically focuses on problems and solutions related to the test-related issues that arise with ICs running at such GHz clock and/or Gbps data rates. GTW'05 will offer a focused forum for experts in the field, as well as for members of the community with a particular interest in this rapidly expanding specialized field.

Areas of interest include but are not limited to

- *Tester architecture and circuitry to provide and support high-speed analog signal sourcing/generation and response capture/sampling*
- *Embedded and internal/external (hybrid) schemes and circuits for sourcing and capturing high speed signals*
- *Low bandwidth testing/testers of GHz/Gbps circuits*
- *Low-cost testing/testers of GHz/Gbps circuits*
- *BIT/BIST for GHz/Gbps circuits*
- *Jitter generation and analysis techniques, and circuitry using embedded, external, and hybrid circuitry*
- *Driving and measuring specifications of I/Os with differential signaling*
- *High-speed/multi-channel test problems and solutions (test fixturing, noise, signal integrity etc)*
- *On-chip infrastructure IP for accurate on-chip timing, voltage, and current measurements*
- *Noise modeling and characterization of channels, cabling, sources, receivers, etc.*
- *Device interface circuitry, and tradeoffs in accuracy and bandwidth*
- *Tradeoffs between yield, ATE overall timing accuracy (OTA), test environment specifications, and I/O timing specifications*
- *DFT and design for manufacturing (DFM) of Gbit/s I/Os*
- *High-speed I/O test power management*
- *Test stimulus and response data transfer and processing, for go/no-go testing and diagnosis*

Author information

To present at the workshop, authors are invited to submit paper proposals. The proposals may be extended abstracts (1,000 words) or full papers. Each submission should include: title, full name and affiliation of all authors, an abstract of 50 words, and keywords. Also, identify a contact author and include a complete correspondence address, phone number, fax number, and e-mail address.

Submit a pdf version of your paper proposal via E-mail. Proposals for panel discussions are also invited. Submissions are due no later than **2 September 2005**.

Submit your paper/panel proposal(s) to Prof. David Keezer, *Georgia Tech.*,
dkeezer@ece.gatech.edu, Tel: +1- 404 894-4741.

Authors will be notified of the disposition of their papers by **23 September 2005**.

Authors of accepted papers may submit an illustrated text by **14 October 2005** for inclusion in the Digest of Papers, which will be provided to the attendees.

GTW'05 is sponsored by the IEEE Computer Society Test Technology Technical Council.

For more information on GTW'05, visit the workshop website at: <http://www.unipi.gr/gtw>

