

# 2<sup>nd</sup> IEEE International GHz/Gbps Test Workshop (GTW'05)

## *Preliminary Program*

### **Thursday, November 10, 2005**

**4:30-5:15PM**

Introductions – Keezer, Chatterjee, Ivanov

Keynote Address

*RF Integrated Systems On Chip: Why SoC + DOT ~ DVM ATE*

*Is The Hottest New RF ATE Technology for 2006 a Digital Voltmeter!?*

Craig Force\*, Texas Instruments

**5:15-6:30PM**

*Tutorial – “Techniques for Measuring High-Speed Switching Noise”*

Karim Arabi\*, PMC Sierra

**7:00-9:00PM**

Reception

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### **Friday, November 11, 2005**

**8:15-9:45AM – Session 2 – GHz Clocking and Picosecond Jitter**

**Moderator: TBD**

*Adventures in Measuring Picosecond Jitter in PLLs and SerDes Transceivers*

Stephen Sunter\*

LogicVision

*GHz-Speed Structural Test Using On-Chip Clocking*

V. Iyengar\*, G. Grise, M. Taylor, R. Farmer

IBM Microelectronics

*Use of Compliant Clock Recovery in Serial Data Test Applications*

S. Fraasch, R. Cook, M. Li\*

Wavcrest Corp.

**9:45-10:15AM**

Coffee Break

**10:15AM-11:45PM – Session 3 - Issues for Testing Multi-Gbps PCI Express**

**Moderator: TBD**

*Test Approach for Multi-Lane PCI Express and HyperTransport Buses Including Synthesized Jitter Injection*

D.C. Keezer, D. Minier, P. Ducharme\*

Georgia Institute of Technology, IBM Canada

*Optimized Method for Pattern Matching of High Speed Devices on ATE*

G. Hansel, K. Stieglbauer\*

Infineon Technologies

*Debugging PCI-Express Functional ATE Test Patterns*

D. Van Dinh, A. Burgmeier, R. Hewlitt, R. Belleau\*

Freescale Semiconductor, Teradyne

**11:45-1:00PM**

Lunch

**1:00-2:30PM – Session 4 – BIST, Delay, Wireless, and RF Testing**

**Moderator: Mani Soma**

*Built-in At-speed Test and Diagnosis of Wireless Transceiver Systems*

D. Han, S. Bhattacharya, A. Halder, and A. Chatterjee\*

Georgia Institute of Technology

*Improved IIP3 Extraction from the Gain Compression Curve*

C. Cho, Y. Ko, W.R. Eisenstadt\*

University of Florida

*Functional Constraints vs. Test Compression in Scan-based Delay Testing*

I. Polian\*, H. Fujiwara

Freiburg University, Nara Institute of Science and Technology

**2:30-3:00PM**

Break

**3:00-4:00PM – Session 5 - Understanding Multi-Gbps Differential Signaling**

**Moderator: TBD**

*A Practical Guide to Lossy Differential Lines*

W. Maichen\*, B. Krsnik

Teradyne, Inc.

*On Differential Signaling and Signal Path for Multi-Gbps DUT I/O and ATE Interface*

M. Shimanouchi

Credance Systems